

**Amendments to the Claims:**

This listing of claims replaces all prior versions, and listings, of claims in this application.

**Listing of Claims:**

1. (Canceled)
2. (Currently Amended) The method of claim [[1]] 11, wherein the first insulating layer comprises an oxide, a nitride, or a combination thereof.
3. (Currently Amended) The method of claim [[1]] 11, wherein the second insulating layer comprises an oxide, a nitride, or a combination thereof.
4. (Currently Amended) The method of claim [[1]] 11, wherein the floating gate is formed with a combination of the reaction gas and a second gas.
5. (Original) The method of claim 4, wherein the reaction gas comprises SiX, wherein X comprises at least one of H<sub>4</sub>, H<sub>2</sub>Cl<sub>2</sub>, HCl<sub>3</sub>, D<sub>4</sub>, D<sub>2</sub>Cl<sub>2</sub>, and D<sub>3</sub>Cl.
6. (Original) The method of claim 4, wherein the reaction gas comprises SiX, Si<sub>2</sub>Y, or a combination of SiX and Si<sub>2</sub>Y.
7. (Original) The method of claim 6, wherein X comprises at least one of H<sub>4</sub>, H<sub>2</sub>Cl<sub>2</sub>, HCl<sub>3</sub>, D<sub>4</sub>, D<sub>2</sub>Cl<sub>2</sub>, and D<sub>3</sub>Cl.
8. (Currently Amended) The method of claim 6, wherein Y comprises at least one of H<sub>6</sub>, H<sub>4</sub>Cl<sub>2</sub>, H<sub>2</sub>Cl<sub>4</sub>, D<sub>6</sub>, D<sub>4</sub>Cl<sub>2</sub>, and D<sub>2</sub>Cl<sub>4</sub>.
9. (Original) The method of claim 4, wherein the second gas comprises one or more of D<sub>2</sub>, H<sub>2</sub>, and D<sub>3</sub>.

10. (Currently Amended) The method of claim ~~[[1]]~~ 11, further comprising forming a plurality of bit lines in the semiconductor substrate.
11. (Currently Amended) ~~The method of claim 1, further comprising~~ A method of forming a semiconductor device, comprising:  
providing a semiconductor substrate;  
forming a first insulating layer over the semiconductor substrate;  
forming a floating gate over the first insulating layer with a reaction gas, wherein the floating gate comprises a microcrystalline material having a grain size of about 50Å-300Å;  
forming a second insulating layer over the floating gate;  
forming a control gate over the second insulating layer; and  
forming a layer of nitride over the control gate layer.
12. (Currently Amended) The method of claim ~~[[1]]~~ 11, further comprising thermally treating the floating gate to increase the grain size of the microcrystalline material to about 200Å-600Å.
13. (Currently Amended) A method of forming a semiconductor device having a memory cell, comprising:  
providing a silicon substrate;  
~~selective~~ selectively doping of the silicon substrate to form a plurality of bit lines in the silicon substrate;  
forming a first insulating layer over the silicon substrate;  
forming a floating gate over the first insulating layer, wherein the floating gate comprises an amorphous material;  
thermally treating the memory cell to transform the amorphous material into a microcrystalline material;  
forming a second insulating layer over the floating gate; and  
forming a control gate over the second insulating layer.

14. (Currently Amended) The method of claim 13, whether the grain size of the microcrystalline material is about  $200\text{\AA}$ - $500\text{\AA}$ .
15. (Original) The method of claim 13, wherein the step of forming the floating gate further comprises depositing the floating gate with a combination of gases, wherein the combination of gases comprise a reaction gas.
16. (Currently Amended) The method of claim 15, wherein the reaction gas comprises  $\text{SiX}$ ,  $\text{Si}_2\text{Y}$ , or a combination of  $\text{SiX}$  and  $\text{Si}_2\text{Y}$ , wherein X comprises at least one of  $\text{H}_4$ ,  $\text{H}_2\text{Cl}_2$ ,  $\text{HCl}_3$ ,  $\text{D}_4$ ,  $\text{D}_2\text{Cl}_2$ , and  $\text{D}_3\text{Cl}$ , and Y comprises at least one of  $\text{H}_6$ ,  $\text{H}_4\text{Cl}_2$ ,  $\text{H}_2\text{Cl}_4$ ,  $\text{D}_6$ ,  $\text{D}_4\text{Cl}_2$ , and  $\text{D}_2\text{Cl}_4$ .
17. (Original) The method of claim 15, wherein the step of forming the floating gate further comprises depositing the floating gate with a combination of the reaction gas and a second gas comprising at least one of  $\text{D}_2$ ,  $\text{H}_2$ , and  $\text{D}_3$ .
18. (Original) The method of claim 13, further comprising forming a layer of nitride over the control gate.
19. (Currently Amended) A method of forming a semiconductor memory device, comprising:
- providing a semiconductor silicon substrate;
  - forming a plurality of bit lines in the silicon substrate;
  - depositing a first insulating layer over the silicon substrate including the plurality of bit lines;
  - forming a floating gate over the first insulating layer, wherein the floating gate comprises one of amorphous material silicon or a microcrystalline material polysilicon having a grain size of  $50\text{\AA}$ - $300\text{\AA}$ ;
  - forming a second insulating layer over the floating gate;
  - forming a plurality of word lines over the second insulating layer; and
  - forming a layer of nitride over the plurality of word lines.

20. (Currently Amended) The method of claim 19, further comprising thermally treating the floating gate so that the floating gate has a grain size of about  $200\text{\AA}$ - $500\text{\AA}$ .
21. (New) The method of claim 11, wherein the floating gate is a polysilicon floating gate.
22. (New) The method of claim 13, wherein the floating gate is a polysilicon floating gate.
23. (New) The method of claim 19, wherein the floating gate is a polysilicon floating gate.